Abstract

[0036] An improved EEPROM device and method for providing a lower device programming voltage is disclosed. An exemplary EEPROM device is configured with a modified drawing layer comprising one or more serrated elements configured underneath a tunneling region of the EEPROM device. The serrated elements can comprise regions having at least one acute angle structure within the active mask drawing layer configured to provide a restriction of the oxygen used to grow the gate oxide that determines the programming voltage of the EEPROM device. In addition the serrated elements can also be configured with at least two acute angle thin oxide regions configured in a staggered arrangement to allow for misalignment between the active layer and the polysilicon layer such that at least one acute angle thin oxide region is found in the tunneling region underneath the polysilicon layer of the tunneling region.. As a result of a thinner gate oxide region being formed, a lower programming voltage is needed by the EEPROM device.